DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Mid Semester Examination – Oct 2018

Course: B. Tech in Computer Engineering/ Information Technology **Sem: III**

Subject Name: Computer Architecture& Organization **Subject Code:**

Max Marks:20 **Date:- 11/10/2018** **Duration:- 1 Hr.**

Instructions to the Students:

1. **All questions are compulsory**
2. **Neat diagrams must be drawn wherever necessary**
3. **Use of calculator is allowed**
4. **Figures to the right indicate full marks**

		(Level/CO)	Marks
Q. 1	**Solc All Questions(Each carry 1 mark)**		**6**
	1. ___ bus decides the range of locations that can be accessed by the processor. a) Data b) Address c) Control d) System	*Remember/CO1*	
	2. Data register in IAS is ___ wide. a) 16 bit b) 40 bit c) 20 bit d) 48 bit	*Remember/CO1*	
	3. In a three address instruction the number of source operand is __ and the number of destination operand is___. a) 2, 1 b)1, 2 c) 3, 0 d) None of the above	*Remember/CO1*	
	4. Identify which of the following is not an addressing mode. a) Stack b) register indirect c) memory indirect d) immediate	*Remember/CO1*	
	5. Which of the following represents the number (-10) in 2s complement format a) 11110110 b) 11011001 c) 00001010 d) 11111100	*Understand/CO1*	
	6. IEEE 754 standard for a single precision representation includes __ bits. a) 16 b) 32 c) 48 d) 64	*Remember/CO1*	
Q.2	**Solve Any Two of the following.**		**3 X 2**
(A)	Differentiate between RISC and CISC architecture.	*Analysis/CO1*	
(B)	Calculate (-7 x 3) using Booths Algorithm.	*Application/CO1*	
(C)	Explain Bus Interconnection.	*Understand/CO1*	
Q. 3	**Solve Any One of the following.**		**8**
(A)	Define addressing modes. List and explain its types	*Remember/CO1*	
(B)	Explain IEEE 754 single precision and double precision format. Represent the number $(-307.1875)_{10}$ in single precision and double precision format.	*Understand/CO1*	

***** End *****