

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Mid Semester Examination – Oct 2018

Course: B. Tech in Computer Engineering

Sem: III

Subject Name: Digital Electronics and Microprocessors

Subject Code: BTCOC305

Max Marks: 20

Date:- 12/10/2018

Duration:- 1 Hr.

Instructions to the Students:

1. All questions are compulsory.
2. Illustrate your answer with suitable diagram and examples.
3. Assume suitable data if required

(Level/CO) Marks
[1 X 6]

Q.1

1. If a signal passing through a gate is inhibited by sending a low into one of the inputs, and the output is HIGH, the gate is a (n):
[A] NAND [B] NOR [C] AND [D] OR [Remember]
2. Convert in to equivalent decimal $2148 = ?$
[A] 10410 [B] 14010 [C] 01410 [D] Not Possible [Understand]
3. Each product term of a group, w'.x.y' and w.y, represents the ____ in that group.
[A] Input [B] Output [C] POS [D] SOP [Apply]
4. Half-adders have a major limitation in that they cannot
[A] No carry output [B] Only one bit addition [Remember]
[C] No carry input [D] None
5. Determine the output frequency for a frequency division circuit that contains 10 flip-flops with an input clock frequency of 20.48 MHz.
[A] 10.24 KHz [B] 5 KHz [C] 30.24 KHz [D] 11.71 KHz [Apply]
6. In a down counter, which flip-flop doesn't toggle when the inverted output of the proceeding flip-flop goes from HIGH to LOW.
[A] MSB F/F [B] LSB F/F [C] All of above [D] None [Understand]

Q.2 Solve any Two of the following.

[2 X 3]

- (A) Encode the data 1001 in even parity, by using Hamming code. [Analyze]
- (B) Minimize given function using K- Map in SOP form
 $F(A, B, C, D) = \sum m(0,3,5,6,7,10,12,13) + \sum d(2,9,15)$ [Analyze]
- (C) Illustrate the working of T flip flop as frequency divider circuit. (Divide by 4) [Apply]

Q.3 Solve any One of the following.

[8 x 1]

- (A) Implement 8:1 Multiplexer using 2:1 Multiplexers. Draw the truth table to justify your answer. [Analyze & Apply]
- (B) Design asynchronous decade counter using T flip-flop. [Analyze & Apply]
