DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD -402 103

Semester Examination – May - 2019

Branch: Electrical Engineering **Sem.:- IV**

Subject with Subject Code: Analog and Digital electronics (BTEEE-406B)

Marks: 60 **Date:-24/05/2019** **Time: 3 Hr.**

Instructions to the Students

1. Each question carries 12 marks.
2. Attempt **any five** questions of the following.
3. Illustrate your answers with neat sketches, diagram etc., wherever necessary.
4. If some part or parameter is noticed to be missing, you may appropriately assume it and should mention it clearly

(Marks)

Q.1. Attempt any 2 from following.

(a) Define AC load line. Draw the AC load line for a Common Emitter configuration amplifier, if $V_{CC} = 20$ V, $R_1 = 16$ KΩ, $R_2 = 4$ KΩ, $R_E = 2$ KΩ, $R_c = 3$ KΩ and $R_L = 12$ KΩ. (6)

(b) In a common emitter amplifier circuit derive the equation for voltage gain A_V. (6)

(c) What is the need of cascading? Derive the gain expression for multistage amplifier. (6)

Q.2. Attempt any 2 from following.

(a) Enlist the characteristics of an ideal OPAMP. Draw the diagram of ideal OPAMP and discuss its functioning. (6)

(b) Define (6)

(i) Input Offset Voltage
(ii) Input Bias Current
(iii) Input impedance

(c) Write a short note on Window Detector using OPAMP. Draw neat circuit diagram and waveforms. (6)

Q.3. Attempt all questions.

(a) Define Universal Gates. Implement using universal gates (6)
(i) AND gate (ii) OR gate.

(b) Convert the following (6)
(i) $(2003.31)_{10} = (\ ?\ )_{16}$ (ii) $(1F0C)_{16} = (\ ?\ )_8$ (iii) $(68.4B)_{16} = (\ ?\ )_8$

Q.4. Attempt all questions.

(a) With appropriate diagram explain the working of CMOS-NOR gate. (6)

(b) Implement a 4-bit Parallel In Serial Out shift register using D Flip Flops (6)

Q.5. Attempt all questions.

(a) Simplify using K-Map f(W,X,Y,Z) = WX'Y'+WY+W'YZ' (6)

(b) Find Prime Implicants for f(W,X,Y,Z) = = Σm (2, 3, 6, ,7, 8, 10, 11, 12, 14, 15) (6)

Q.6. Attempt any 2 from following.

(a) Implement 4-bit Ripple Carry Adder. (6)

(b) Design a full subtractor circuit using 3:8 Deoder (6)

(c) Write a short note on diode switch matrix. (6)

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